

# NTHS5445T1

## Power MOSFET P-Channel ChipFET™

### 5.2 Amps, 8 Volts

#### Features

- Low  $R_{DS(on)}$  for Higher Efficiency
- Logic Level Gate Drive
- Miniature ChipFET Surface Mount Package Saves Board Space

#### Applications

- Power Management in Portable and Battery-Powered Products; i.e., Cellular and Cordless Telephones and PCMCIA Cards

#### MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	5 secs	Steady State	Unit
Drain-Source Voltage	$V_{DS}$	-8.0		V
Gate-Source Voltage	$V_{GS}$	$\pm 8.0$		V
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) (Note 1.) $T_A = 25^\circ\text{C}$ $T_A = 85^\circ\text{C}$	$I_D$	$\pm 7.1$ $\pm 5.2$	$\pm 5.2$ $\pm 3.7$	A
Pulsed Drain Current	$I_{DM}$	$\pm 20$		A
Continuous Source Current (Note 1.)	$I_S$	-2.1	-1.1	A
Maximum Power Dissipation (Note 1.) $T_A = 25^\circ\text{C}$ $T_A = 85^\circ\text{C}$	$P_D$	2.5 1.3	1.3 0.7	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150		$^\circ\text{C}$

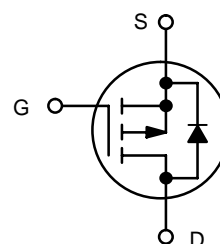
1. Surface Mounted on 1" x 1" FR4 Board.



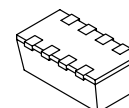
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**5.2 AMPS**  
**8 VOLTS**  
 **$R_{DS(on)} = 35 \text{ m}\Omega$**

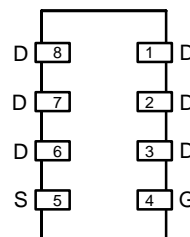


P-Channel MOSFET

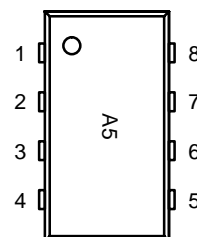


ChipFET  
CASE 1206A  
STYLE 1

#### PIN CONNECTIONS



#### MARKING DIAGRAM



A5 = Specific Device Code

#### ORDERING INFORMATION

Device	Package	Shipping
NTHS5445T1	ChipFET	3000/Tape & Reel

# NTHS5445T1

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
Maximum Junction-to-Ambient (Note 2.) $t \leq 5$ sec Steady State	$R_{thJA}$	40 80	50 95	$^{\circ}C/W$
Maximum Junction-to-Foot (Drain) Steady State	$R_{thJF}$	15	20	$^{\circ}C/W$

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
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### Static

Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250 \mu A$	-0.45	-	-	V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0 V, V_{GS} = \pm 8.0 V$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -6.4 V, V_{GS} = 0 V$	-	-	-1.0	$\mu A$
		$V_{DS} = -6.4 V, V_{GS} = 0 V,$ $T_J = 85^{\circ}C$	-	-	-5.0	
On-State Drain Current (Note 3.)	$I_{D(on)}$	$V_{DS} \leq -5.0 V, V_{GS} = -4.5 V$	-20	-	-	A
Drain-Source On-State Resistance (Note 3.)	$r_{DS(on)}$	$V_{GS} = -4.5 V, I_D = -5.2 A$	-	0.030	0.035	$\Omega$
		$V_{GS} = -2.5 V, I_D = -4.5 A$	-	0.040	0.047	
		$V_{GS} = -1.8 V, I_D = -2.0 A$	-	0.052	0.062	
Forward Transconductance (Note 3.)	$g_{fs}$	$V_{DS} = -5.0 V, I_D = -5.2 A$	-	18	-	S
Diode Forward Voltage (Note 3.)	$V_{SD}$	$I_S = -1.1 A, V_{GS} = 0 V$	-	-0.8	-1.2	V

### Dynamic (Note 4.)

Total Gate Charge	$Q_g$	$V_{DS} = -4.0 V, V_{GS} = -4.5 V,$ $I_D = -5.2 A$	-	17	26	nC
Gate-Source Charge	$Q_{gs}$		-	2.8	-	
Gate-Drain Charge	$Q_{gd}$		-	2.6	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -4.0 V, R_L = 4 \Omega$ $I_D \cong -1.0 A, V_{GEN} = -4.5 V,$ $R_G = 6 \Omega$	-	15	25	ns
Rise Time	$t_r$		-	45	70	
Turn-Off Delay Time	$t_{d(off)}$		-	110	165	
Fall Time	$t_f$		-	65	100	
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = -1.1 A, di/dt = 100 A/\mu s$	-	30	60	

2. Surface Mounted on 1" x 1" FR4 Board.
3. Pulse Test: Pulse Width  $\leq 300 \mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production testing.

TYPICAL ELECTRICAL CHARACTERISTICS

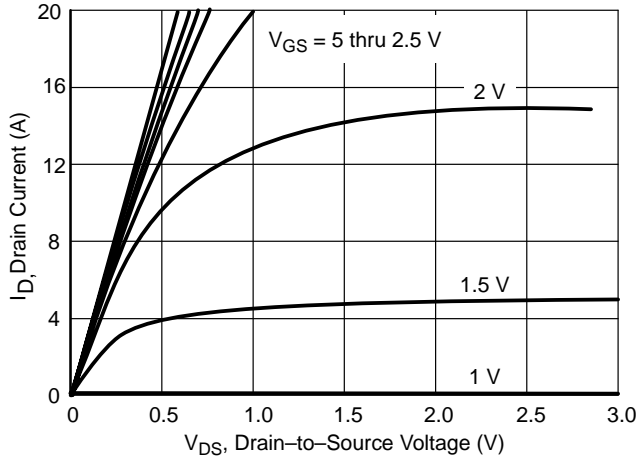


Figure 1. Output Characteristics

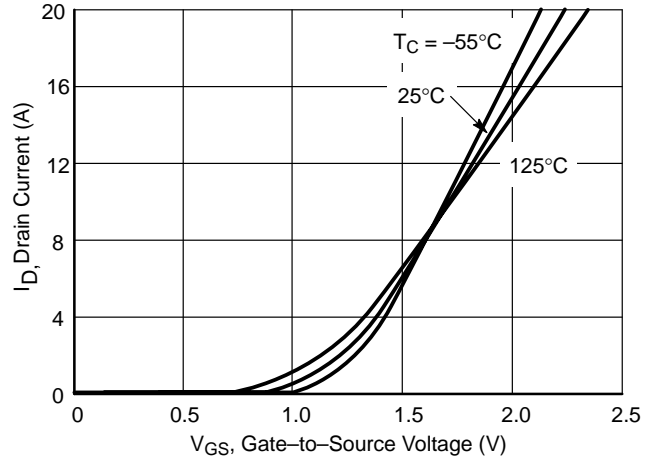


Figure 2. Transfer Characteristics

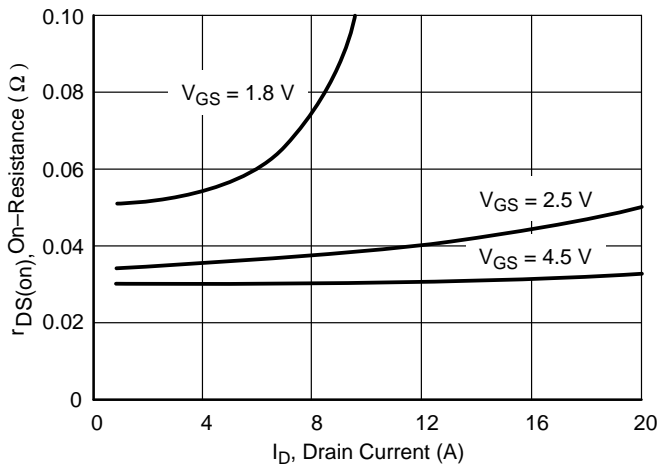


Figure 3. On-Resistance vs. Drain Current

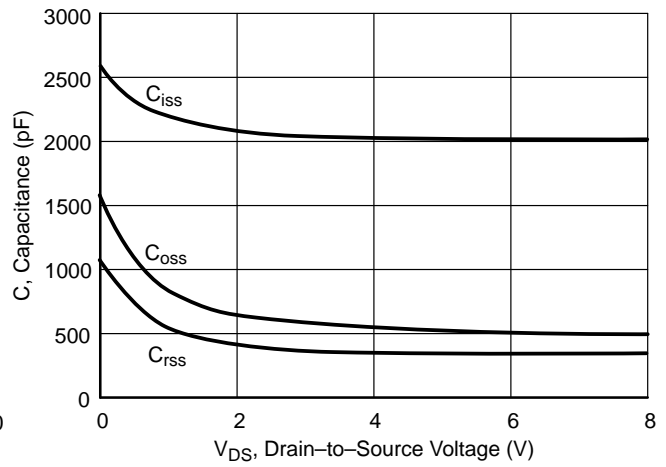


Figure 4. Capacitance

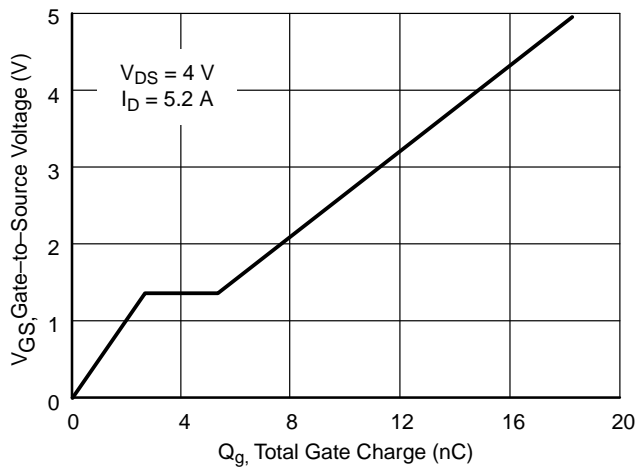


Figure 5. Gate Charge

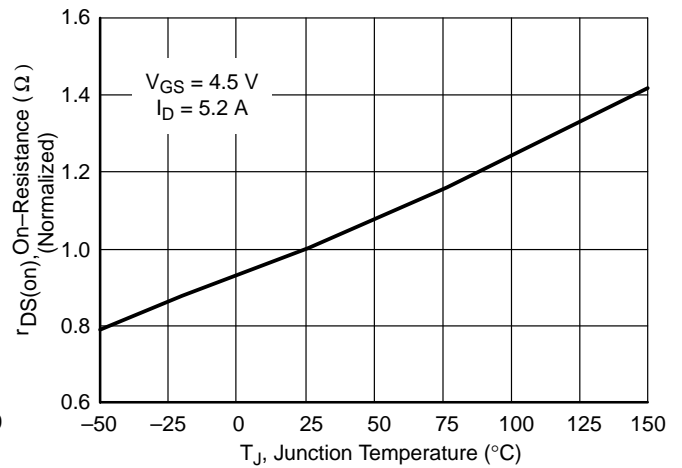


Figure 6. On-Resistance vs. Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

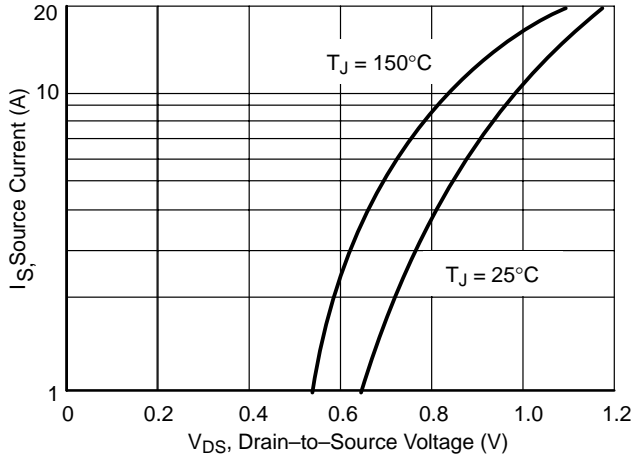


Figure 7. Source-Drain Diode Forward Voltage

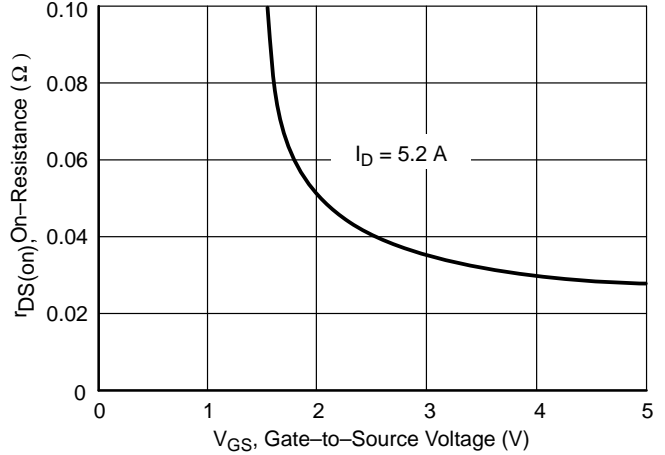


Figure 8. On-Resistance vs. Gate-to-Source Voltage

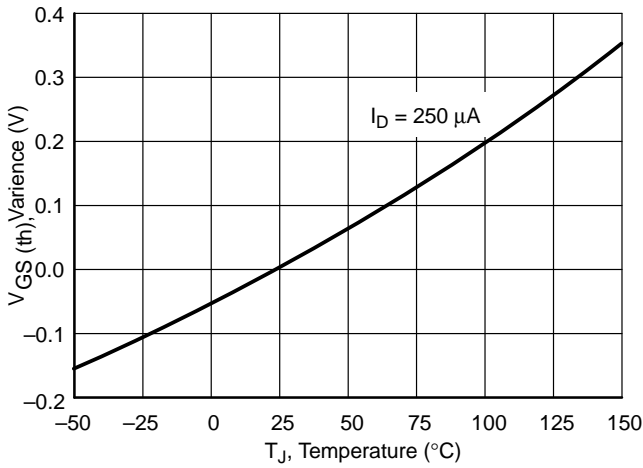


Figure 9. Threshold Voltage

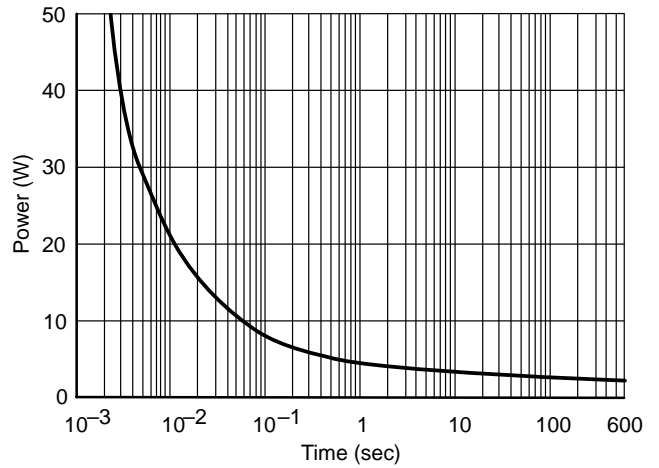


Figure 10. Single Pulse Power

TYPICAL ELECTRICAL CHARACTERISTICS

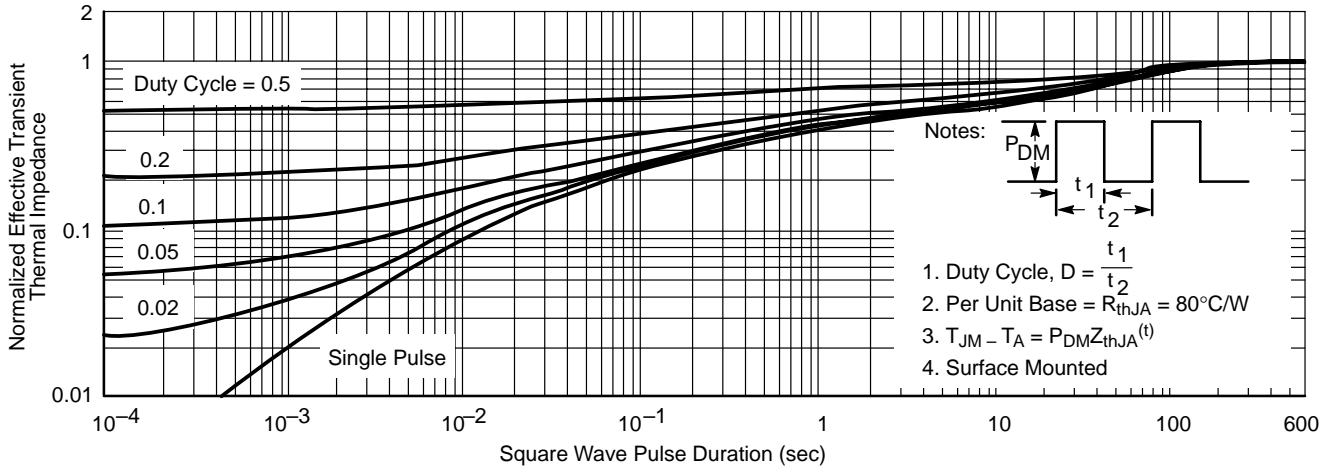


Figure 11. Normalized Thermal Transient Impedance, Junction-to-Ambient

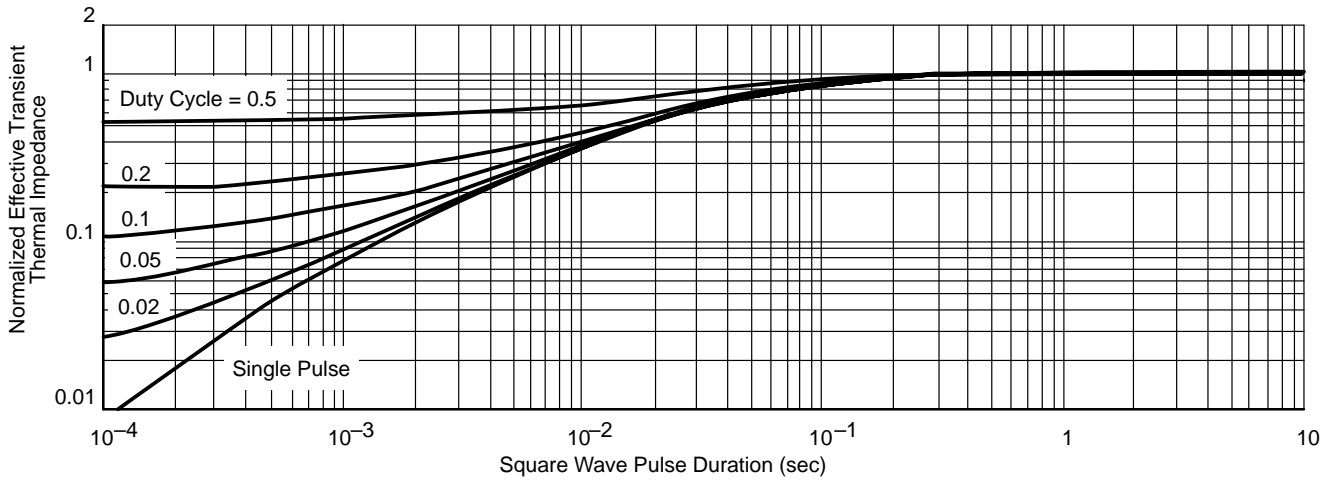
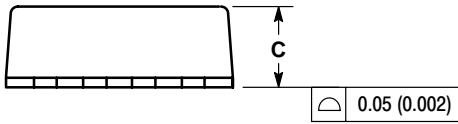
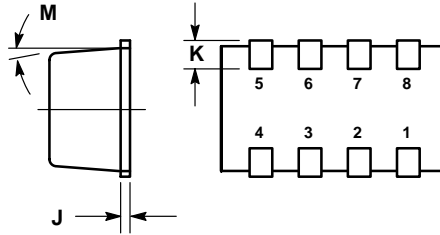
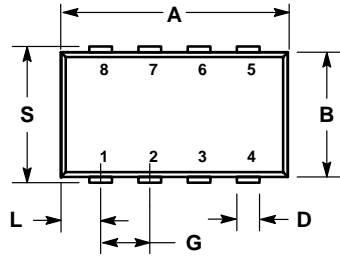


Figure 12. Normalized Thermal Transient Impedance, Junction-to-Foot

# NTHS5445T1

## PACKAGE DIMENSIONS

### CHIPFET CASE 1206A-01 ISSUE A



- STYLE 1:  
 PIN 1. DRAIN  
 2. DRAIN  
 3. DRAIN  
 4. GATE  
 5. SOURCE  
 6. DRAIN  
 7. DRAIN  
 8. DRAIN

#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.95	3.10	0.116	0.122
B	1.55	1.70	0.061	0.067
C	1.00	1.10	0.039	0.043
D	0.25	0.35	0.010	0.014
G	0.65 BSC		0.025 BSC	
J	0.10	0.15	0.004	0.008
K	0.30	0.45	0.012	0.018
L	0.55 BSC		0.022 BSC	
M	5 ° NOM		5 ° NOM	
S	---	1.80	---	0.071

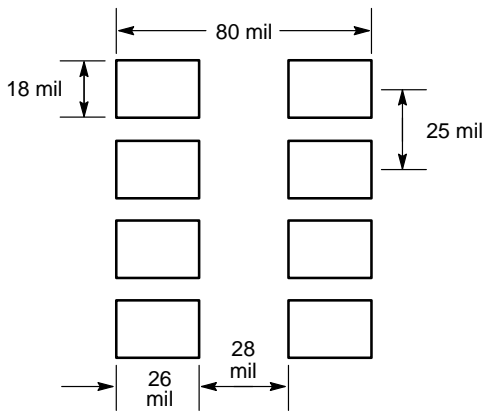


Figure 13.

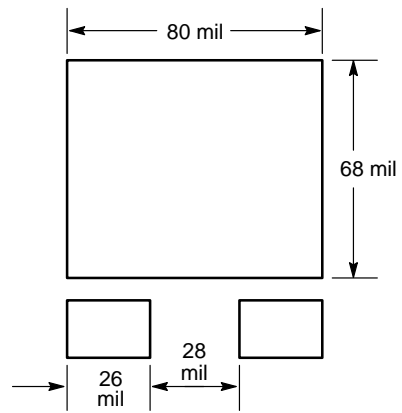


Figure 14.


**BASIC PAD PATTERNS**

The basic pad layout with dimensions is shown in Figure 14. This is sufficient for low power dissipation MOSFET applications, but power semiconductor performance requires a greater copper pad area, particularly for the drain leads.

The minimum recommended pad pattern shown in Figure 13 improves the thermal area of the drain connections (pins 1, 2, 3, 6, 7, 8) while remaining within the

confines of the basic footprint. The drain copper area is 0.0054 sq. in. (or 3.51 sq. mm). This will assist the power dissipation path away from the device (through the copper leadframe) and into the board and exterior chassis (if applicable) for the single device. The addition of a further copper area and/or the addition of vias to other board layers will enhance the performance still further.

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